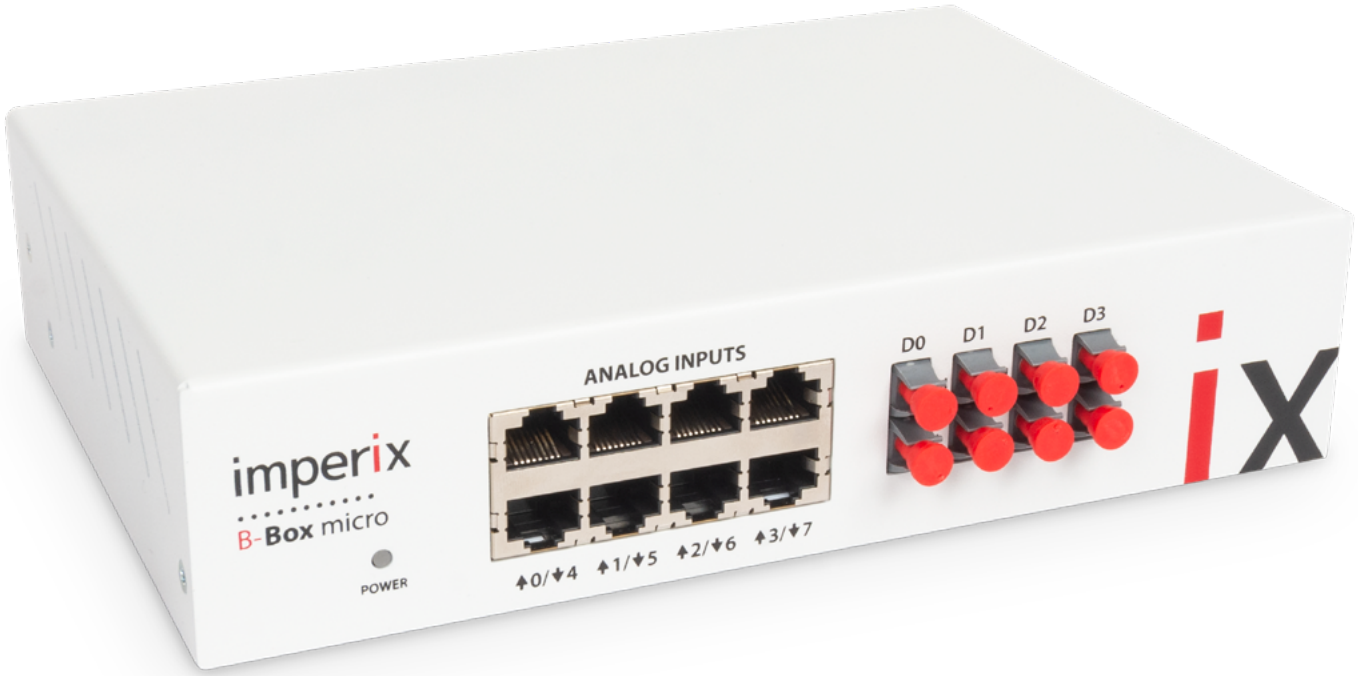
B-Box Micro

Desktop converter controller

The B-Box Micro is the little brother of the B-Box RCP. Despite its limited I/Os , it shares the same heart, making it ideal for entry-level power electronic applications, such as in teaching environments.



GENERAL DESCRIPTION

The B-Box Micro is a digital controller which is designed as an intermediate solution between the regular-sized B-Box RCP controller and the Evaluation Kit for B-Board PRO. In terms of functionality, the B-Box Micro features the same capabilities as the Evaluation Kit, but with plug-&play connectivity for imperix power modules as well as with imperix current and voltage sensors.

TYPICAL APPLICATIONS

With its 8 analog input channels, 8 PWM output channels and digital I/Os, the B-Box Micro is able to control a three-phase grid-connected inverter or other systems of similar complexity. Besides, the controller is easily programmable either with conventional C/C++ control development, or using Simulink / PLECS. Therefore, the B-Box Micro is perfectly suited for educational applications as in teaching of power electronics.

KEY FEATURES AND SPECIFICATIONS

- Dual-core 1 GHz ARM processor
- User-programmable FPGA (Kintex-grade)
- Up to 2 MSPS sampling frequency
- Up to 250 kHz closed loop control frequency
- Advanced pulse-width modulators (PWM)
- Plug-&-play with imperix voltage / current sensors
- Small form factor

I/O CAPABILITIES

- 8x analog inputs (±5 V)
- 8x optical PWM outputs
- 8x digital outputs (5 V)
- 16x digital inputs (8x 5 V, 8x 3.3 V)
- Fully-configurable input / output bus (36 pins)

FRONT AND BACK PANEL

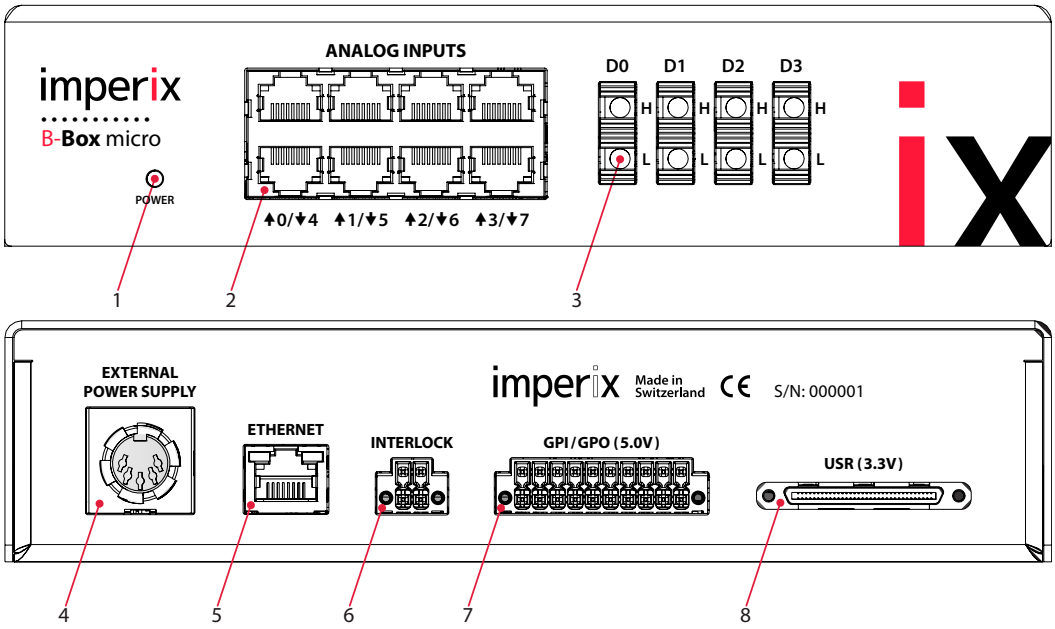


Fig. 1. Front and back panel views of the B-Box Micro.

1) Power LED
2) Analog inputs (RJ45, ±5 V)
3) PWM outputs (PWM lanes #0-#7)
4) Power supply
5) Ethernet port (RJ45)
6) Electrical interlock connector (IN/OUT)
7) Digital inputs and outputs (5 V)
8) VHDCI connector, USR pins (3.3 V)

MAIN SPECIFICATIONS

Component	Specification
System on chip	*Xilinx Zynq XC7Z030-3FBG676E*
Processing system	*ARM Cortex A9 1 GHz x2* *1GB DDR3*
Programmable logic (FPGA)	*Kintex 7 125K (user programmable)*
Storage	*Flash 16 MB x2* *micro SD + eMMC 8 GB*
Communication	*Ethernet 1 Gbps x1*
Analog inputs	*16 bits, simultaneous sampling x8* *2 Msps (maximum speed)*
PWM outputs	*Optical 50 Mbps x8* *Various modulators* *4 ns resolution*
User High-speed I/Os	*FPGA direct (3.3 V) x36*
General-purpose digital inputs (GPI)	*Electrical (5 V / 3.3 V) x8 / x8*
General-purpose digital outputs (GPO)	*Electrical (5 V) x8*
Fault inputs / outputs	*Electrical interlock (5 V) x1*
Incremental decoder inputs	*3-pins (A,B,Z) x4* *Shared with GPI inputs*

Table 1. Main system specifications for B-Box Micro.

DEVICE CONTENT

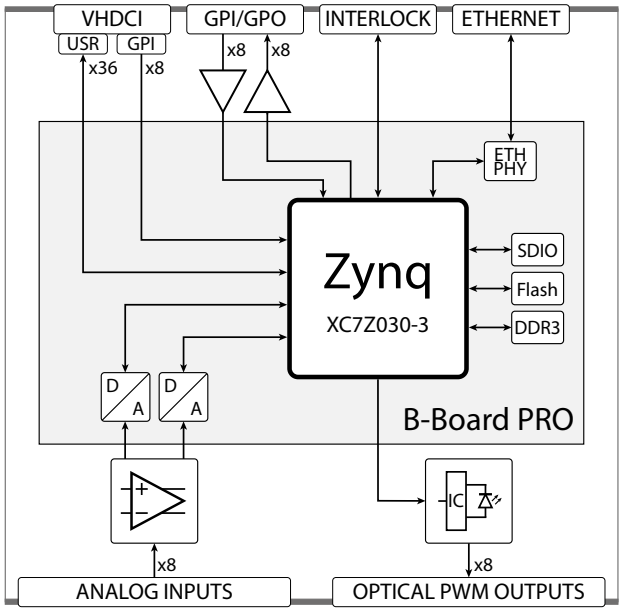


Fig. 2. Simplified system description of B-Box Micro.

LOGICAL STRUCTURE

The B-Box Micro operates thanks to an association between two CPU cores and dedicated peripherals implemented in programmable logic. The distribution of tasks is as follows:

- CPU0: Running on Linux, the first core is responsible for loading the application code, supervising the system execution and managing the data logging.
- CPU1: Running on BBOS (lightweight secured proprietary operating system), the second core executes the application-level control code developed by the user.
- FPGA: The programmable logic area contains all the application-specific peripherals. By default, the corresponding firmware is fixed.

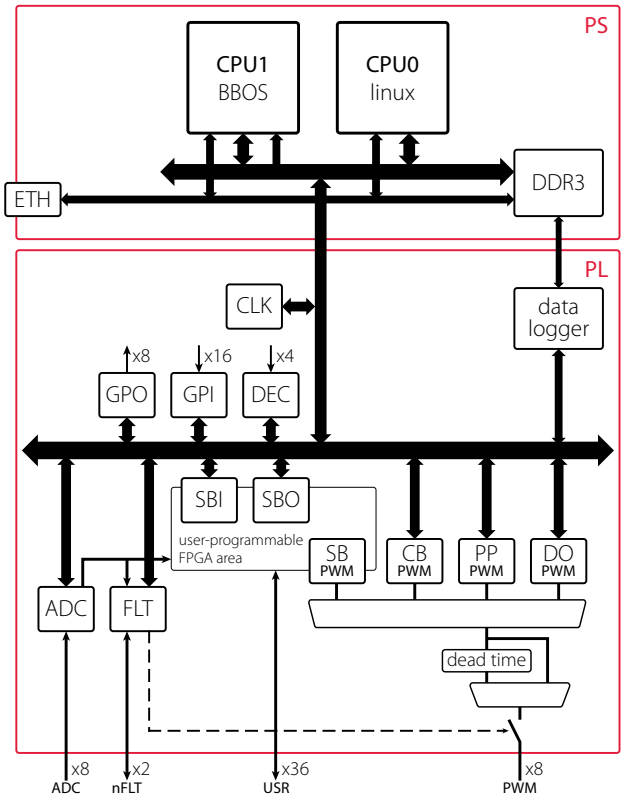


Fig. 3. Functional overview of the B-Box Micro.

The pre-implemented FPGA peripherals are as follows:

- CLK: Offers clock generators with up to four separate time-bases that can be used with other peripherals.
- ADC: Acquires data from the 8 analog input channels located on board.
- SBI: Provides easy-to-use access for inbound data traffic from the user-programmable area (sandbox).
- SBO: Provides easy-to-use access for outbound data traffic from the user-programmable area (sandbox).
- DEC: Support the decoding of signals produced by up to four incremental encoders for motor drive applications.
- CB-PWM: Contains 8 fully-configurable carrier-based modulators (conventional sampled PWM).
- PP-PWM: Provides hardware support for the generation of Programmed Patterns. It is useful for PWM techniques such as Selective Harmonic Elimination (SHE) or Optimized Pulse Patterns (OPP) in general.
- DO-PWM: Offers a Direct Output operation, allowing to force a specific lane state (0 or 1). This is useful for control techniques such as Model Predictive Control (MPC) or Direct Torque Control (DTC).
- SB-PWM: Provides access to the PWM outputs from the user-programmable area (sandbox).
- GPO: Offers 8 General-Purpose Outputs.
- GPI: Offers 16 General-Purpose Inputs.
- FLT: Handles the fault signals and safety limits of the analog inputs.
- USR: Provides a direct access to the 36 fully-configurable high-speed I/O lanes.
- ETH: Supports data exchanges on Ethernet (TCP/UDP).

ANALOG INPUTS

The B-Box Micro features an analog front-end with 8 input channels as in Fig. 4. A-to-D conversion is achieved with the LTC2324-16 full-differential analog-to-digital converters on B-Board PRO. The analog inputs on the B-Box Micro do not feature protection thresholds on the hardware-level, but it is possible to configure safety limits in the programmable logic area (see page 6).

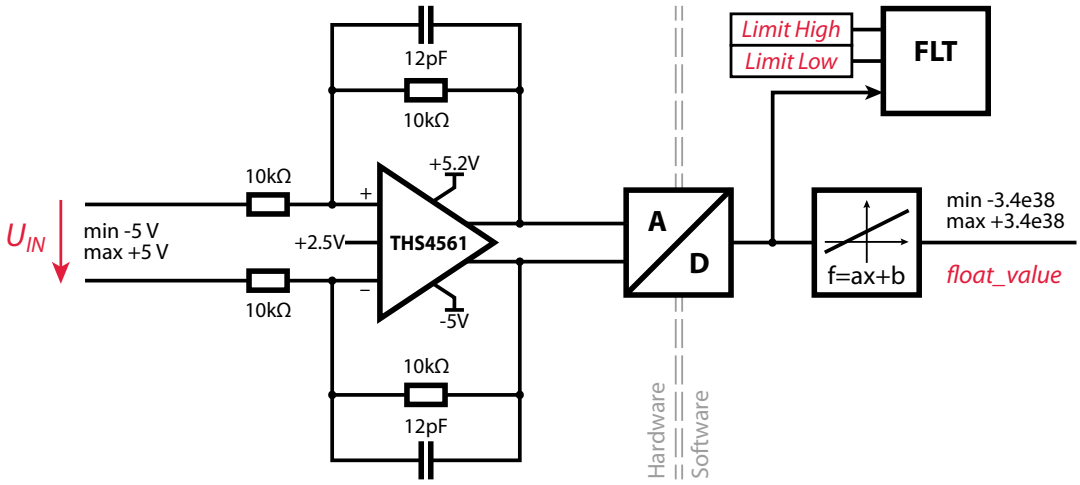


Fig. 4. Block diagram of each channel of the analog input front-end.

Characteristic	Test conditions	Min.	Typ.	Max.	Unit
Input voltage range	*Differential*		*±5.0*		*V*
	Common mode		*±4.5*		*V*
Max tolerable voltage	*On any analog input pin*			*±7.0*	*V*
Input impedance		*19.98*	*20.0*	*20.02*	*kΩ*
Signal bandwidth	*-3 dB*		*1.3*		*MHz*
CMRR	*0 Hz – 10 kHz*		*>83*		*dB*
	100khz		*>67*		*dB*
	>1 Mhz		*>50*		*dB*
Noise	*RMS*		*0.24*	*0.38*	*mV*
Offset			*±0.4*	*±0.8*	*mV*
Precision / Gain error			*±0.6*	*±1.1*	*%*
Embedded power supply voltage	*directly from external power supply*		*±15*		*V*
Embedded power supply output current	*per channel*			*140*	*mA*

Table 2. Overall performance specifications of the analog front-end (each channel).

Analog inputs rely on RJ45 connectors. This allows the use of well shielded twisted pair cables for the connection to sensors, with a good EMI performance. The +15 V and -15 V outputs supply the connected sensors. Internally they are protected with a PTC fuse for every +/-15 V output.

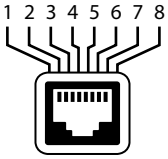


Fig. 5. RJ45 connector pin assignment.

Pin	Pair	Color	Description
1	*2*	*orange stripe*	*+15 V output*
2	*2*	*orange solid*	*+15 V output*
3	*3*	*green stripe*	*0 V*
4	*1*	*blue solid*	*Positive input*
5	*1*	*blue stripe*	*Negative input*
6	*3*	*green solid*	*0 V*
7	*4*	*brown stripe*	*-15 V output*
8	*4*	*brown solid*	*-15 V output*

Table 3. Pinout of the analog inputs.

OPTICAL OUTPUTS

PWM lanes #0 to #7 are available on optical fiber outputs. They rely on FT50MHNR transmitters from Firecomms. By default, two consecutive PWM lanes are associated to form a PWM channel. Several configurations of PWM channels are possible, similarly to electrical PWM outputs:

- PWMH + PWML: high- and low-side gate drive signals, i.e. pseudo-complimentary signals with a configurable dead time between their '1' states. In this case two PWM lanes form a PWM channel.
- PWM + ACTIVE: PWM and switching authorization signals, i.e. one switching signal and one for blocking / unblocking the operation. In this case, two PWM lanes also form a PWM channel.
- INDEPENDENT: each PWM lane is linked to its own PWM modulator. In this case, no PWM channel is formed and dead time is not enforced.

In pseudo-complimentary mode (PWMH + PWML), a dead time can be freely configured by software.

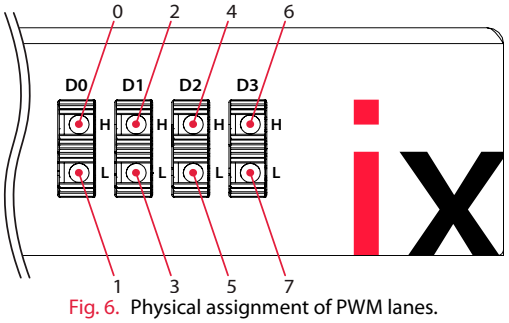


Fig. 6. Physical assignment of PWM lanes.

The timings of the optical outputs are shown in Table 4.

Characteristic	Test conditions	Min.	Typ.	Max.	Unit
Wavelength		*640*	*650*	*670*	*nm*
Propagation delay asymmetry	*Any two signals, 3σ*			*± 13*	*ns*
Relative jitter (optic)	*Any two signals, 3σ*			*± 1.8*	*ns*

Table 4. Performance specifications of the optical PWM outputs.

FAULT INTER-LOCKING SIGNALS

Fault inter-locking allows to coordinate emergency mechanisms between a B-Box Micro and other appliances. The fault output nFLT_OUT is high as long as no fault condition is active. Accordingly, nFLT_IN must be driven high externally during normal operation. To indicate a fault condition, nFLT_IN must be tied to GND. When a fault occurs, PWM outputs are blocked. The connector is part number 1787014 from Phoenix Contact and the mating part is 1790292.

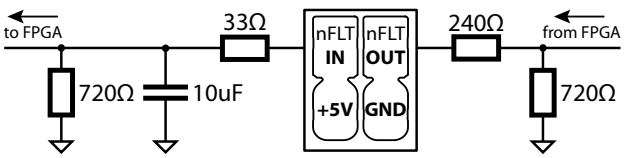


Fig. 9. Circuit for the inter-locking mechanism.

DIGITAL INPUTS AND OUTPUTS

The digital outputs are driven by the translating transceiver 74LVCH8T245, which shifts the output voltage up to +5 V. Reciprocally, the same approach is used for the inputs, as shown in Fig. 7.

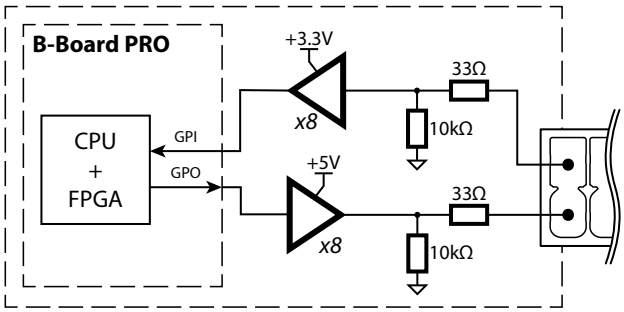


Fig. 7. Digital inputs and outputs circuit.

The pinout of the digital inputs and outputs is shown from the outside perspective in Fig. 8. Additionally to the digital inputs and outputs, there are three GND as well as a +5 V output. The +5 V output is protected using a resettable PTC fuse with a hold current of 140 mA. The connector is part number 1787098 from Phoenix Contact. The mating part is 1790373.

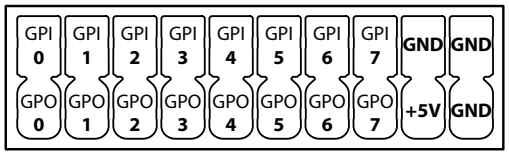


Fig. 8. Pinout of the GPIO connector.

Characteristic	Min	Typ	Max	Unit
GPI input voltage, high level	*3.5*		*5.5*	*V*
GPI input voltage, low level			*1.5*	*V*
GPO rise/fall time		*25*		*ns*
GPO output current			*50*	*mA*
+5 V output current			*140*	*mA*

Table 5. Specifications of digital inputs and outputs.

Characteristic	Min.	Typ.	Max.	Level
Operating voltage		*5.0*		*V*
Response delay to blocking of PWM signals	*0.58*		*13.19*	*ms*

Table 6. Performance specifications of inter-locking mechanism.

Additionally, fault signals are available on the VHDCI connector on a logic level of 3.3 V, as shown in Fig. 10. Because the fault input on the VHDCI connector is pulled high internally, there is no need to drive it actively.

VHDCI

The VHDCI connector (part number : Molex 5796055-1) on the rear side of the device offers the following functions.

- GPI : General purpose inputs (8 bits)
- USR : Fully-configurable input / output bus (32+4 bits)
- FLT : Input and output
- 3.3 V : Total ouput current max. 140 mA

The pinout is the same as the digital inputs connector (B) on B-Box RCP.

Pins	Signal	Level
1, 10, 19, 28, 34, 35-44, 53, 62, 68	*GND*	
2-9	*GPI 8-15*	*3.3 V*
11-18, 20-27	*USR 0-15*	*3.3 V*
45-52, 54-61	*USR 16-31*	*3.3 V*
29-32	*USR 32-35*	*3.3 V*
63-66	*3.3 V*	
33	*nFLT_IN*	*3.3 V*
67	*nFLT_OUT*	*3.3 V*

Table 7. Pinout of VHDCI connector.

The B-Box Micro features a high-speed bus of 36x bidirectional I/Os that is directly accessible from the user-programmable area (inside the Zynq chip). This area, also designated as sandbox offers easy-to-use access from / to the processing cores through the dedicated SBI and SBO blocks.

Characteristic	Min.	Typ.	Max.	Level
Operating data bitrate (all lanes)			*400*	*Mbps*
Operating voltage	*3.0*	*3.3*	*3.6*	*V*

Table 8. Performance specifications of the USR bus.

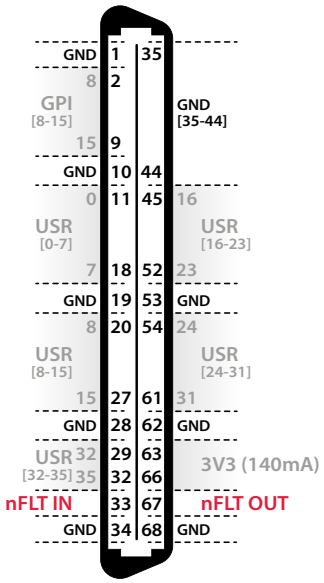


Fig. 10. Pinout of VHDCI connector.

FAULT MANAGER

At the firmware level, all fault signals are grouped inside the fault manager, which manages the overall system execution state and controls the activation of the PWM outputs. The collected fault signals include:

- nFLT_IN (2x)
- Safety limits on analog inputs AIN 0..7

The wachdog counter (WDG) is automatically configured with a period of 2.5 times the control processing period. A fault is raised when no data is received by FPGA logic within this interval.

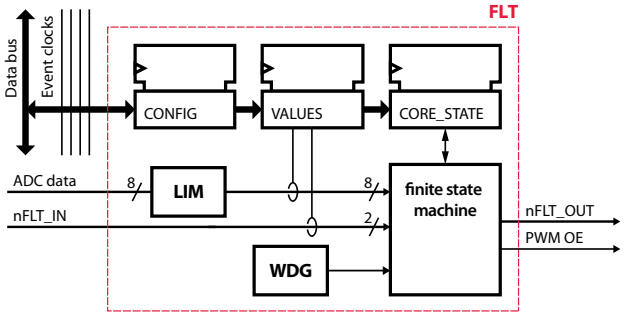


Fig. 11. Internal structure of the FLT peripheral block.

For each analog input channel a low and high safety limit can be set in software. When either of these thresholds is crossed, the PWM signals are instantly blocked and the B-Box Micro sets to FAULT state.

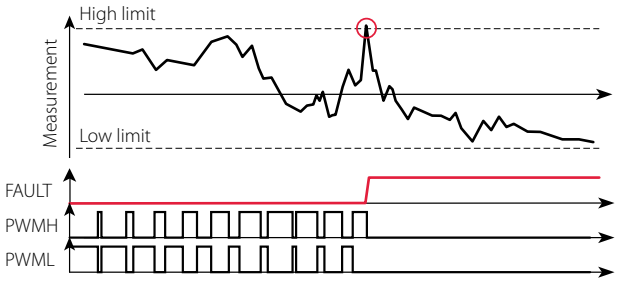


Fig. 12. Operating principle of the safety limits.

Characteristic	Min.	Typ.	Max.	Level
Configurable range		*±5.0*		*V*
Setting resolution		*0.1*		*V*
Response delay to blocking of PWM signals		*2.0*	*4.0*	*µs*

Table 9. Performance specifications of the programmable safety limits.

CLOCK AND INTERRUPT GENERATORS

Four independent clock generators are available on B-Box Micro. They allow to configure independent time bases that can be allocated to various FPGA peripherals. This guarantees a very strict management of frequencies and phase-shifts between blocks. Clock generators support glitch-less re-configuration during run-time (variable-frequency).

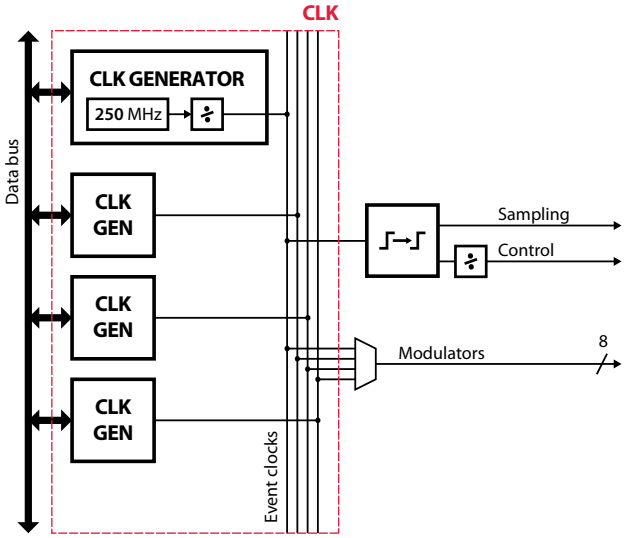


Fig. 13. Internal structure of the CLK peripheral block.

Outputs of clock generators are either interrupt signals or reference clocks for pulse-width modulators. Typical configurations include:

» Basic example: Control, modulation and sampling are at the same frequency. All resources are mapped onto the same clock generator. Measurements are made in the middle of the current ripple.

» Multi-frequency example: Two distinct converters are switching at different frequencies (e.g. 4 kHz and 5 kHz). Sampling is done at a common multiple (e.g. 20 kHz).

» Variable-frequency: One variable-frequency generator is used for modulation. Another frequency generator is used at a constant frequency for sampling and control.

Characteristic	Value
Counter resolution	*4.0 ns*
Counter depth (carrier, prescaler)	*16 bits*
Postscaler value (IRQ subsystem)	*0 – 4095*
Achievable frequency range	*58.2 mHz – 250 MHz*

Table 10. Performance specifications of the CLK peripheral block.

PULSE WIDTH MODULATORS

The B-Box Micro embeds a full PWM signal generation system, featuring four sub-systems. Fig. 14 depicts the corresponding structure:

» CB-PWM: Carrier-based modulators (4 channels with complementary signals). Various types of carriers are available, with single or double update rate. The CB-PWM block also provides hardware support for space-vector modulation (SV-PWM).

» DO-PWM: Direct outputs. The direct access to the output state ('1' or '0') typically enables the implementation of software-modulated techniques such as Model Predictive Control (MPC). This also allows to use PWM outputs as standard digital outputs (possibly with dead time).

» PP-PWM: Programmed patterns modulators (three-phase). They allow the implementation of Selective Harmonic Elimination (SHE) or other types of Optimized Pulse Patterns (OPP).

» SB-PWM: This subsystem connects with the user-programmable area (sandbox), which allows for the implementation of fully-customized modulation techniques. Easy-to-use I/O access from the software level is offered by the SBI and SBO blocks (see page 10).

At the output, each of the 8 PWM signals can be directly propagated to the physical outputs or to go through a dead time generator.

This results in 8 PWM lanes. By default, lanes are also arranged into 4 pairs of adjacent lanes designated as channels. Within a channel, odd lanes are always low-side signals, while even lanes are always high-side.

Dead time is obtained by delaying the rising edge of each PWM signal within a given pair. This results in an equivalent propagation delay of half the dead time.

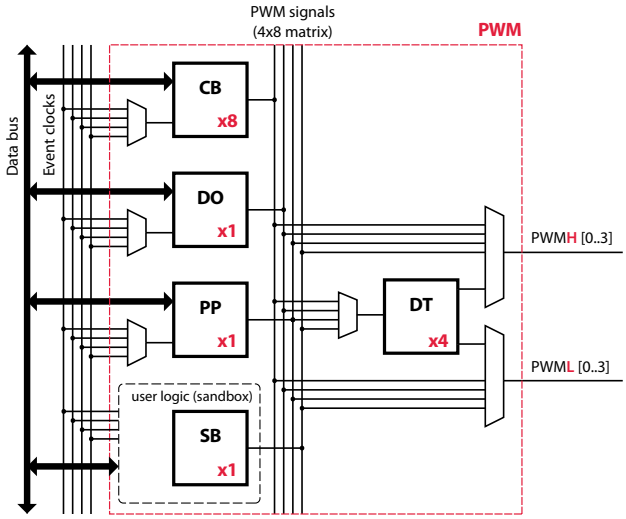


Fig. 14. Internal structure of the PWM signals generation block.

CB-PWM : CARRIER-BASED MODULATION

Carrier-based modulators offer the simplest way to generate pulse-width modulated signals. The corresponding subsystem features 4 independent modulators with complementary outputs. Each modulator offers independent duty-cycle and phase parameters as well as four different types of carriers. With triangular carriers, modulators can be configured with single or double update rates (once or twice per PWM period).

Characteristic	Min.
Counter depth	*16 bits*
Edge resolution (counter resolution)	*4 ns*

Table 11. Performance specifications of the CB-PWM block.

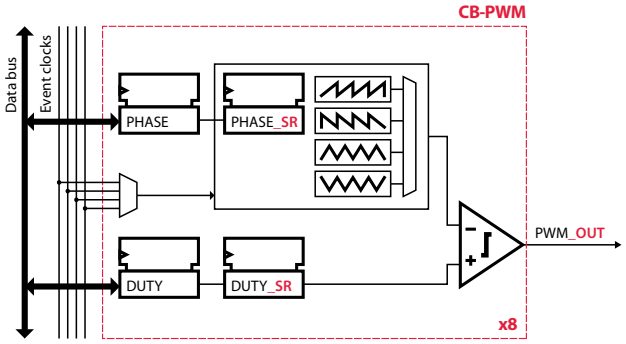


Fig. 15. Internal structure of the CB-PWM peripheral block.

SV-PWM : SPACE VECTOR MODULATION

Space vector modulation (sometimes referred to as SVM) is supported through dedicated software drivers, making use of the same resources as the CB-PWM subsystem. Indeed, once the closed vectors have been identified and the suitable sequence determined, the switching events can be easily produced by suitably-programmed modulators.
SV-PWM automatically configures adjacent channels and supports single or double update rates.

DO-PWM : DIRECT OUTPUT ACCESS

Direct access to the PWM outputs is supported by the DO-PWM subsystem. It distinguishes from the SB-PWM in the sense that it is pre-implemented and requires no HDL editing. PWM state values (0 or 1) can be written directly from the CPU cores. This may typically be useful for model-predictive control (MPC) or sliding mode control techniques such as direct torque control (DTC).
Similarly to all PWM subsystems, when used as a channel, output lanes benefit from the dead-time generator block as well as protective mechanisms.

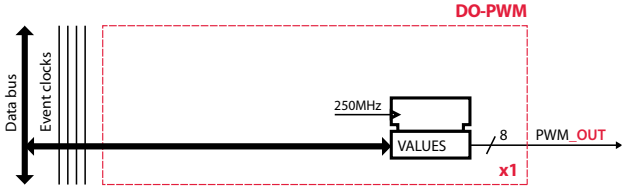


Fig. 16. Internal structure of the DO-PWM block.

PP-PWM : PROGRAMMED PATTERNS MODULATION

The programmed pattern blocks support modulation techniques that rely on pre-defined switching instants such as the generation of firing angles on a thyristor-based converter, the implementation of Selective Harmonic Elimination (SHE) or any Optimized Pulse Pattern (OPP). Three-phase system are supported.
PP-PWM have a fixed counter period (hence angular resolution), but can nevertheless be fed by variable-frequency clocks (see CLK peripheral block), typically aiming to be integrated within a software PLL.
The PP-PWM block contains several look up tables (LUT) for switching angles, registers for indicating the direction (up or down) of each switching event, as well as an additional truth table for decoding the output state.
The PP-PWM block is meant for accelerating the run time execution of OPP-based modulation and not for supporting the computation of the associated optimization algorithms.

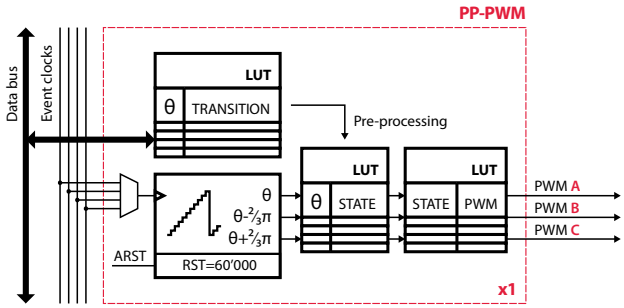


Fig. 17. Internal structure of the PP-PWM block.

Characteristic	Value
Number of angle registers (values 0 – 60'000)	*3x 16 angles x 16 bits*
Number of transition direction bits registers (up or down)	*3x 16 bits*
Edge resolution (respectively to signal period)	*0.017 ‰*

Table 12. Performance specifications of the PP-PWM block.

SB-PWM : PWM ACCESS FROM THE SANDBOX

In addition to existing modulators, the B-Box Micro also features a user-programmable area inside the FPGA . This notably allows to implement special own modulation techniques.
In this sandbox, data read and write access from / to the CPU is provides from the the SBI and SBO blocks, respectively (see "User-programmable area (Sandbox)" on page 10).
The SB-PWM subsystem itself allows to connect to the PWM lanes through the dead-time generator block (see Fig. 14).

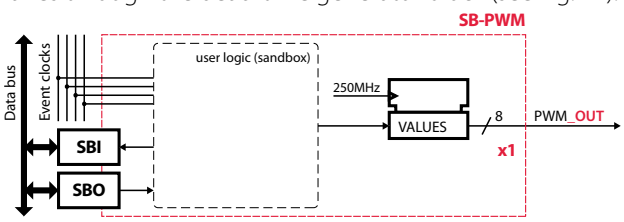


Fig. 18. Internal structure of the SB-PWM block.

DEAD TIME GENERATION SUBSYSTEM

As depicted by Fig. 14, the PWM block features a dead time generator at its output. This subsystem can be either used or bypassed by picking-up the signals from the PWM signals matrix directly (outputs of the modulators). Signals from all four PWM subsystems can be routed to the physical outputs (optical).

The dead time generation relies on a finite state machine operating as depicted in Fig. 19. Essentially, rising edges of the high-side and low-side signals are delayed by a programmable amount of time. This results in an equivalent propagation delay of half the dead time.

Intrinsically, this implementation guarantees that a pulse shorter than the dead time value is not produced.

Characteristic	Min.	Typ.	Max.	Unit
Dead time resolution		*4*		*ns*
Dead time value	*0.004*		*262*	*µs*

Table 13. Performance specifications of the dead time generation.

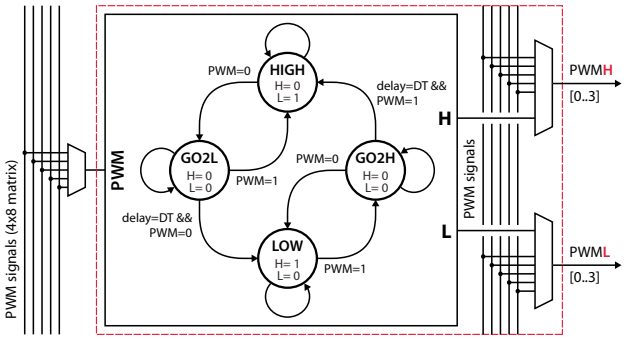


Fig. 19. Internal structure of the dead time generation block.

INCREMENTAL POSITION DECODERS

The B-Box Micro features decoder inputs for quadrature-encoder speed / position sensor signals (usually called A and B), with or without a reset line (usually called Z). These inputs are either configurable as four independent inputs or two differential inputs.

Each decoder module counts all 4 edges of the A and B inputs, leading to an angular resolution 4 times superior to the PPR value usually specified for a given encoder. The position counter can be reset either at a specified value, or using the Z signal provided by the sensor.

Finally, the position can be latched similarly and simultaneously to the sample and hold feature of the ADC inputs, or simply read at the start of the data transfers to the CPU.

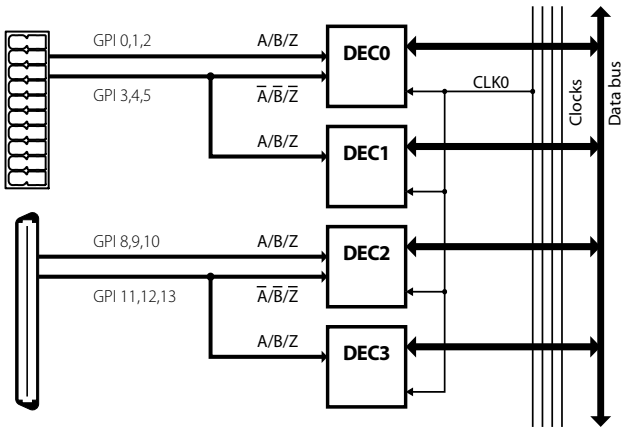


Fig. 20. Device mapping and configuration of the four incremental speed / position sensors decoders.

Characteristic	Test conditions	Min.	Typ.	Max.	Unit
Input signals	• *Single-ended signalling: A, B and Z (Z is optional)* • *Differential signalling: A, $\overline{A}$, B, $\overline{B}$, Z, $\overline{Z}$ ($\overline{Z}$ are optional)*				
Sampling options	*Either synchronized with ADC, or independent*				
PPR frequency	*Quadruple rate.*	*0*		*5*	*MHz*

Table 14. Performance specifications of the DEC block.

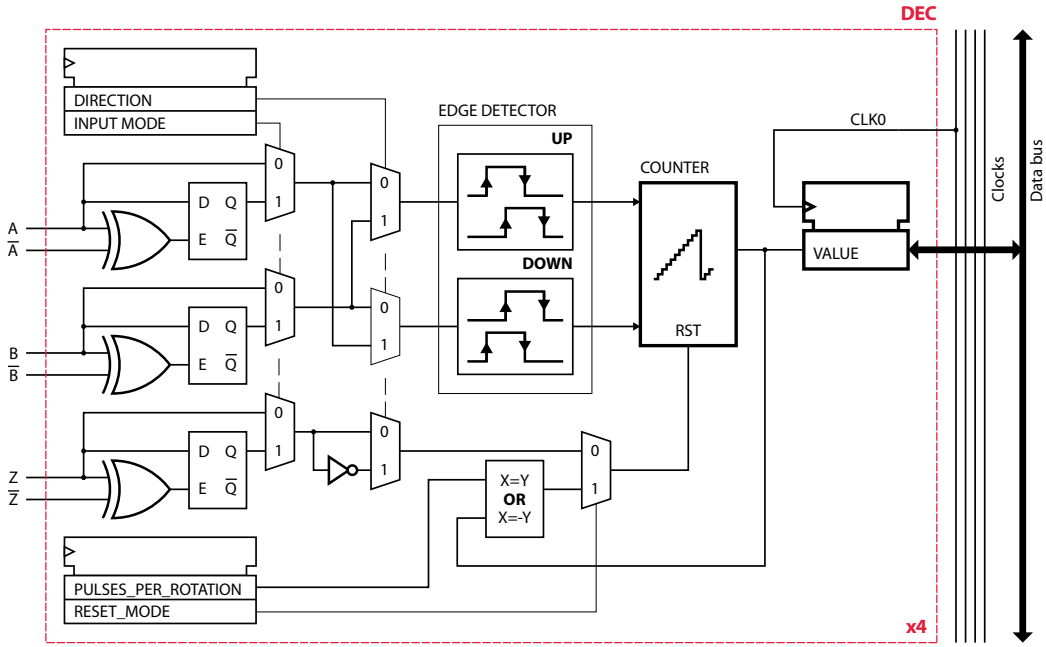


Fig. 21. Internal structure of the DEC block.

USER-PROGRAMMABLE AREA (SANDBOX)

The B-Box Micro is designed such that its programmable logic area (PL) can embed user-defined logic. This may allow for the implementation of special modulation techniques, proprietary communication mechanisms, or interfacing with external hardware and components.

Within this special area, designated as *sandbox*, two peripheral blocks are pre-implemented for easy-to-use I/O access from / to the CPU cores :

» SBI : Input from the sandbox
» SBO : Output to the sandbox

Also, the sandbox offers connectivity to the following I/O :

» ADC values (8x 16 bits signed integers)
» SB-PWM signals (32 bits register)
» Internal clocks
» Physical I/Os (FLT, USR, GPI, GPO)

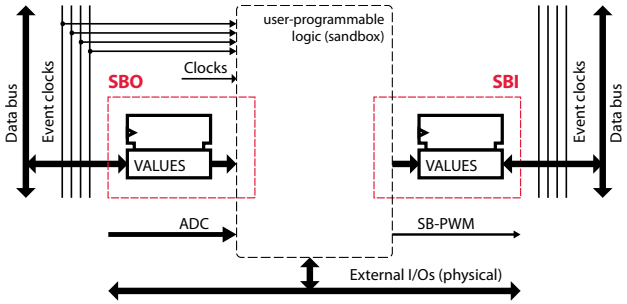


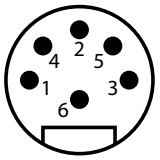
Fig. 22. Internal structure of the SBI and SBO blocks.

C/C++ drivers (as well as their blockset counterparts) are readily available within the software development kits (SDKs). On the programmable logic side, development templates are provided upon request. In the provided HDL source code, other peripheral blocks are obfuscated.

> WARNING:
> The sandbox gives access to all FPGA resources of the B-Board, including some that are not available on the B-Box Micro (SS-PWM, etc) or with a limited number of channels (ADC, PWM etc.).

POWER SUPPLY

The B-Box Micro requires external power supply of +5V / +15V / -15V. The recommended power supply unit is XP Power AEH45UM32. The pinout of the main power supply connector is given below, its part number is 5212044-1.



Pin1 GND
Pin2 GND
Pin3 +5V
Pin4 -15V
Pin5 +15V
Pin6 GND

Fig. 23. Pinout power supply connector.

MECHANICAL DATA

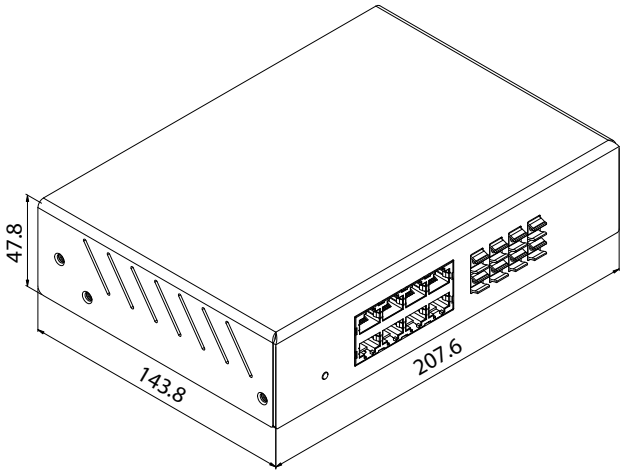


Fig. 24. Mechanical dimensions (in mm) of B-Box Micro.

INCLUDED ACCESSORIES

The B-Box Micro includes the following accessories:

- Ethernet cable (3m): To program and monitor the B-Box Micro from a PC.
- Single-phase power cord (2m): For auxiliary power. The plug's type depends on the destination country.
- Power supply unit: The recommended power supply XP Power AEH45UM32 is delivered with the B-Box Micro.
- GPIO connector: The part number of the GPIO connector is 1787098 and its mating part (delivered with the B-Box Micro) is 1790373.
- Interlock connector: The part number of the interlock connector is 1787014 and its mating part (delivered with the B-Box Micro) is 1790292.

SOFTWARES

Programming the embedded controller requires either the ACG SDK (automated code generation from Simulink and PLECS), or the CPP SDK (C/C++). The corresponding licenses are sold separately.
Please note that the capability to edit the FPGA firmware and the real-time monitoring software (imperix Cockpit) are included in both SDKs, and do not require any additional license.

This product must be used in electric/electronic equipment with respect to applicable standards and safety requirements in accordance with the manufacturer's operating instructions.
Caution, risk of electrical shock! When using the devices, certain parts of the modules may carry hazardous voltages (e.g. power supplies, busbars, etc.). Disregarding this warning may lead to injury and/or cause serious damage. All conducting parts must be inaccessible after installation.

REVISION HISTORY

- 22.12.23: Preliminary version
- 14.02.24: Initial release

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ABOUT US

Imperix Ltd is a company established in Sion, Switzerland. Its name is derived form the Latin verb imperare, which stands for controlling and refers to the company's core business: the control of power electronic systems. Imperix commercializes hardware and software solutions related to the fast and secure implementation of pilot systems and plants in the field of power conversion, energy storage and smart grids.

NOTE

While every effort has been made to ensure accuracy in this publication, no responsibility can be accepted for errors or omissions.
Data may change, as well as legislation, and the reader is strongly advised to obtain copies of the most recently issued regulations, standards, and guidelines.